Zynq UltraScale+ RFSoC Power Delivery

April 4, 2018

Simple, Easy Solutions™

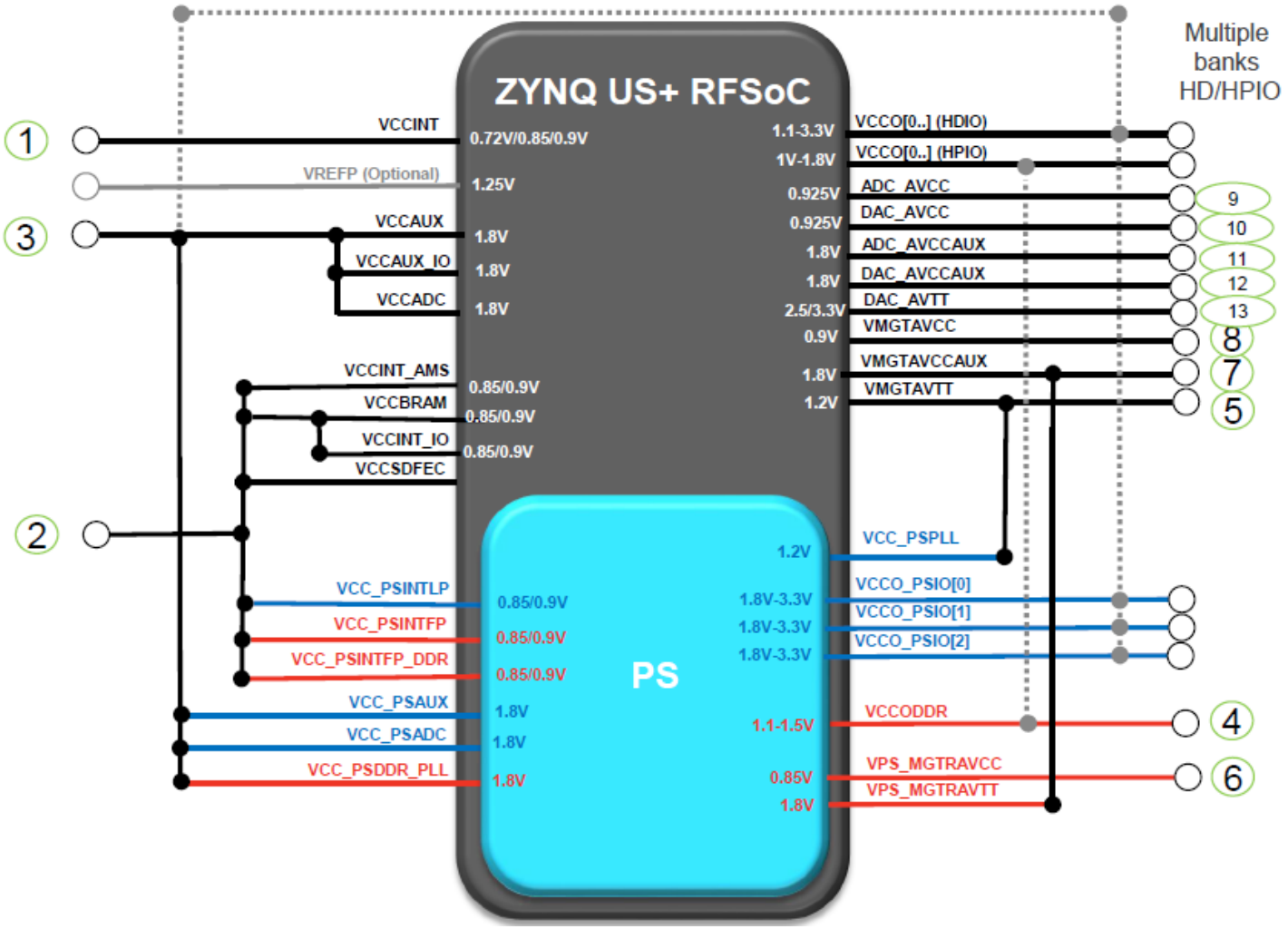
rev 20170706

Zynq UltraScale+ RFSoC Power Rails

Vin=12V

Rail#	Rail	Voltage	Ripple (DC+AC)	Load	Step Load	Comments
1	VCCINT	0.72/0.85/ 0.9V	±3%	30-45A	25%	Assume up to 100A/us 25% load steps
2	VCCBRAM/INT_IO /INT_AMS/SDFEC	0.85/0.9V	±3%	10-20A	40-70%	Assume 40% for ZU25/27/29DR Assume70% for ZU21/28DR
3	VCCAUX/ADC/IO VCC_PSAUX/DDR_PLL/ADC	1.8V	±3%	1.6-2A	90%	Additional current may be needed for 1.8V IO
4	VCCO_PSDDR DDR_VDDQ	1.1-1.5V	DDR	DDR	DDR	Powervendor use their expertise to for this rail
5	VMGTAVTT VCC_PSPLL/VCU_PLL	1.2V	±3%	2-4A	25%	10mV pk-pk ripple at FPGA pins. See UG578
6	VPS_MGTRAVCC	0.85V	±3%	0.3A	50%	10mV pk-pk ripple at FPGA pins. See UG578
7	VPS_MGTRAVTT VMGTVCCAUX	1.8V	±3%	0.1-0.5A	25%	10mV pk-pk ripple at FPGA pins. See UG578
8	VMGTAVCC	0.9V	±3%	1-2A	25%	10mV pk-pk ripple at FPGA pins. See UG578
9	ADC_AVCC	0.925V	±3%	1.7-2A	20%	50uV rms0.1-100kHz, 0.25mV pk-pk ripple 0.1-15MHz
10	ADC_AVCCAUX	1.8V	±3%	1.2-1.3A	20%	10mV pk-pk0.1-15MHz
11	DAC_AVCC	0.925V	±3%	1.1-2.2A	20%	50uV rms0.1-100kHz, 0.4mV pk-pk ripple 0.1-15MHz
12	DAC_AVCCAUX	1.8V	±3%	0.25-0.5A	20%	2mV pk-pk ripple 0.1-15MHz
13	DAC_AVTT	2.5 or 3.0V	±3%	0.3-0.6A	20%	8mV pk-pk ripple 0.1-15MHz
14	VCCO	User	±5%			

Zynq UltraScale+ RFSoC Power Rail Consolidation



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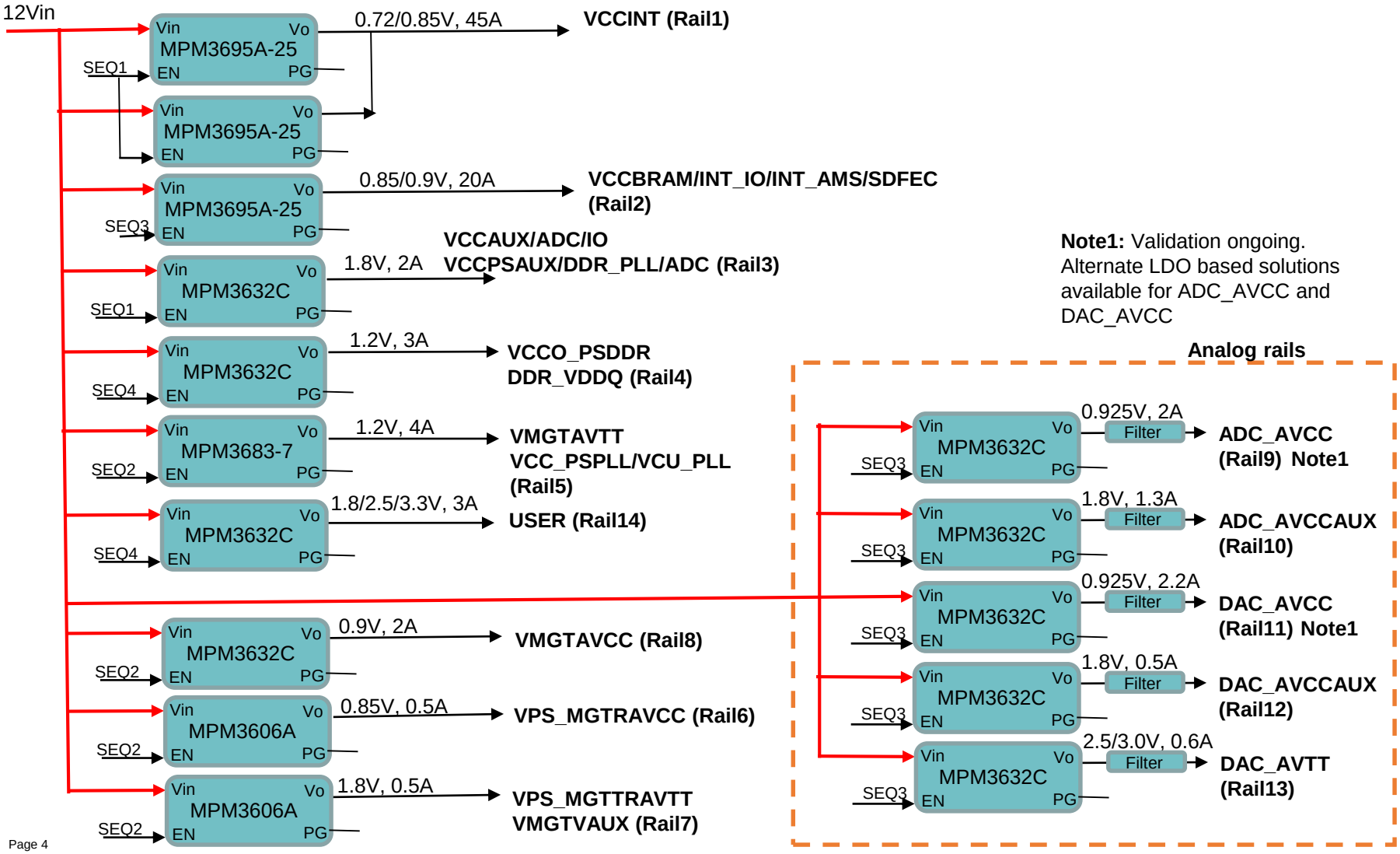
Zynq UltraScale+ RFSoC – Module solution



Note1: Validation ongoing. Alternate LDO based solutions available for ADC_AVCC and DAC_AVCC

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Key Features Zynq UltraScale+ RFSoC (using modules)

	VIN 12V +/-5%									
Rail#	Rail	VOUT	Ripple	Load	Step Load	Seq Up/Dwn	MPS Part#		pcb Area (mm2)	Efficiency @ 50% load
1	VCCINT	0.72/0.85/0.9V	+/-3%	30-45A	25%	1/4	MPM3695A-25 (2x)		426	89.00%
2	VCCBRAM/INT_IO /INT_AMS/SDFEC	0.85/0.9V	+/-3%	10-20A	40-70%	3/2	MPM3695A-25 (1x)		230	88.00%
3	VCCAUX/ADC/IO VCC_PSAUX/DDR_PLL/ADC	1.8V	+/-3%	1.6-2A	90%	1/4	MPM3632C		55	85.00%
4	VCCO_PSDDR DDR_VDDQ	1.1-1.5V	+/-3%	3A	25%	4/1	MPM3632C		55	80.00%
5	VMGTAVTT VCC_PSPLL/VCU_PLL	1.2V	+/-3%	2-4A	25%	2/3	MPM3683-7		80	89.00%
6	VPS_MGTRAVCC	085V	+/-3%	0.5A	50%	2/3	MPM3606A		35	78.00%
7	VPS_MGTRAVTT VMGTVCCAUX	1.8V	+/-3%	0.1-0.5A	25%	2/3	MPM3606A		35	65.00%
8	VMGTAVCC	0.9V	±3%	1-2A	25%	2/3	MPM3632C		55	78.00%
14	VCCO	User (1.8/2.5/3.3V)	±5%	3A max	25%	4/1	MPM3632C		55	90.00%
9	ADC_AVCC	0.925V	±3%	1.7-2A	20%	3/2	MPM3632C		55	80.00%
10	ADC_AVCCAUX	1.8V	±3%	1.2-1.3A	20%	3/2	MPM3632C		55	85.00%
11	DAC_AVCC	0.925V	±3%	1.1-2.2A	20%	3/2	MPM3632C		55	80.00%
12	DAC_AVCCAUX	1.8V	±3%	0.25-0.5A	20%	3/2	MPM3632C		55	82.00%
13	DAC_AVTT	2.5 or 3.0V	±3%	0.3-0.6A	20%	3/2	MPM3632C		55	88.00%
								sq mm	1301	
							Total	sq in	2.02	87.0%

Efficiency 87%, size 2.0sqin

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Overview – Zynq UltraScale+ RFSoC Proposals

- 12Vin design (no intermediary regulator required)
- Design can be easily scaled/modified for customer requirements
- Common use of parts allow step and repeat for ease of design

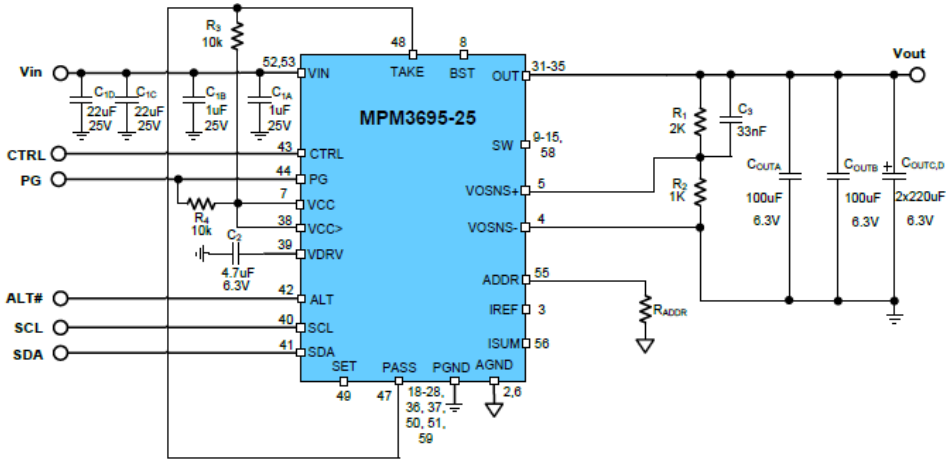
- Smallest size, Minimum Engineering effort
  - Easy to use 2x Parallelable modules (40A VCCINT) for high efficiency and fast transient response
  - MPM modules are fully factory tested solutions and require minimum engineering
  - MPM modules include inductors
  - Total system efficiency ~87%
  - Total solution size ~2.0 sqin including input & output Caps

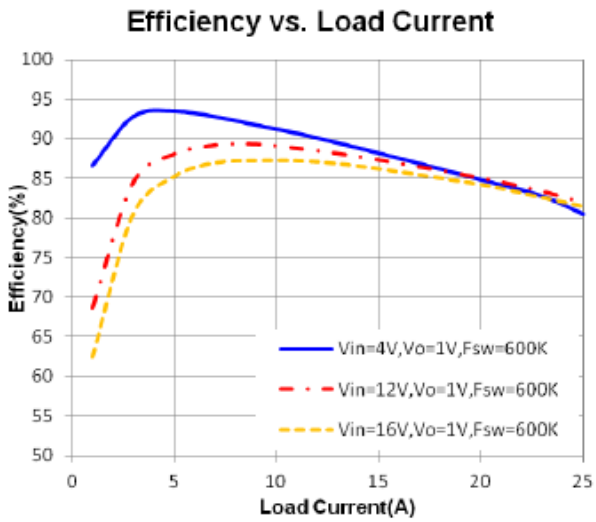
Design details

- Modules with integrated Inductors
  - MPM3695A-25 (25A scalable module)
  - MPM3683-7 (7A module)
  - MPM3732C (3A module)
  - MPM3606A (0.6A module)

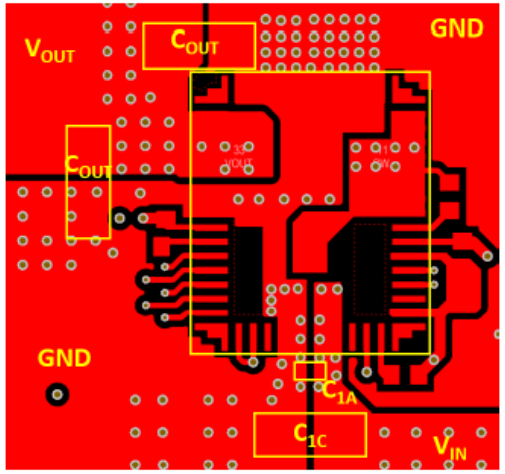
MPM3695A-25

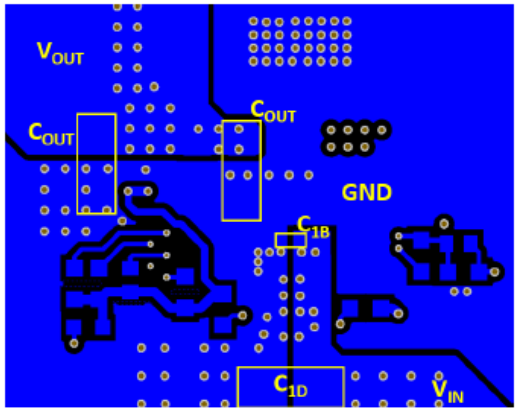
Schematics





Layout guidelines





Solution size: 230mm2

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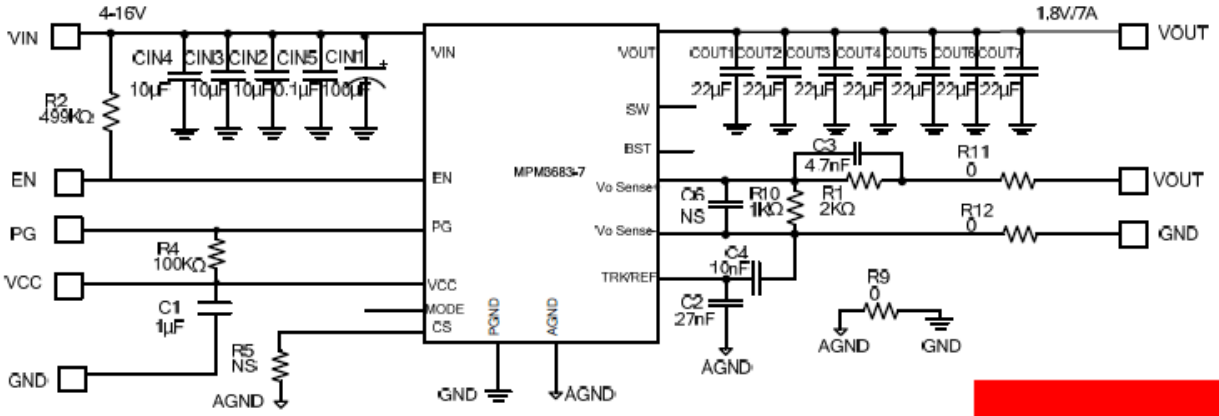
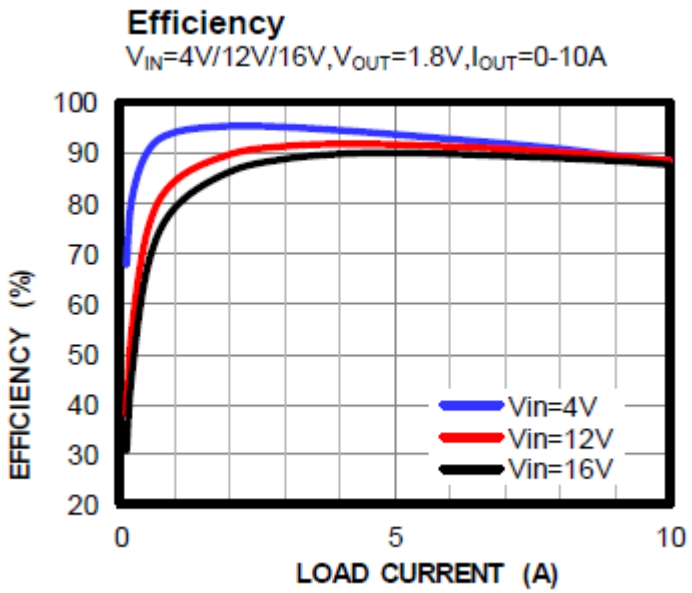
MPM3683-7

Schematics





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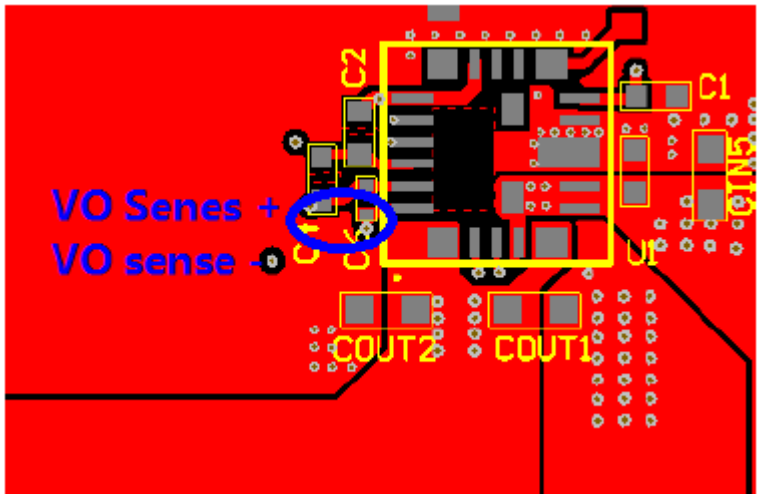

Solution size: 80mm2

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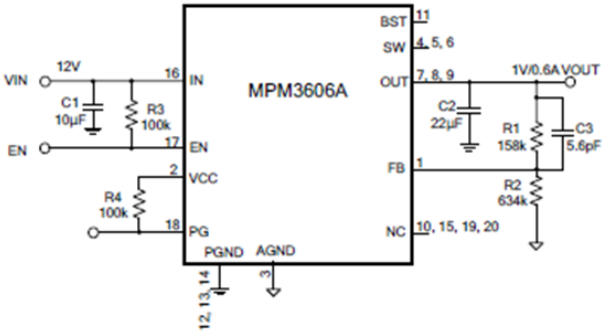
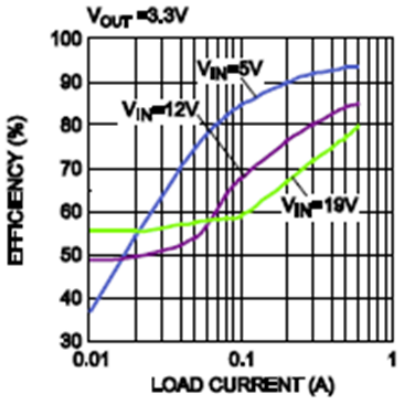
MPM3606A

Schematics (Typical)





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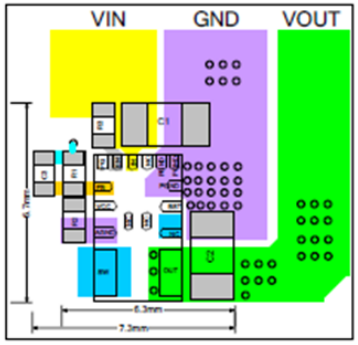
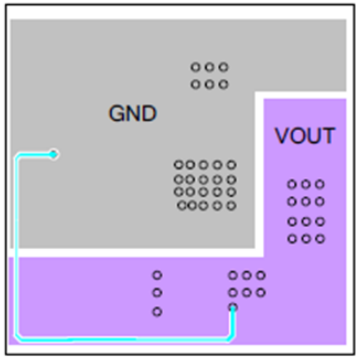


Top Layer



Bottom Layer

- Solution footprint: 32mm^2
- External Components:7

Caps included in area calculations:

Output Caps 1x 22uF 0805

Input Caps: 2x 0603 on PCB bottom

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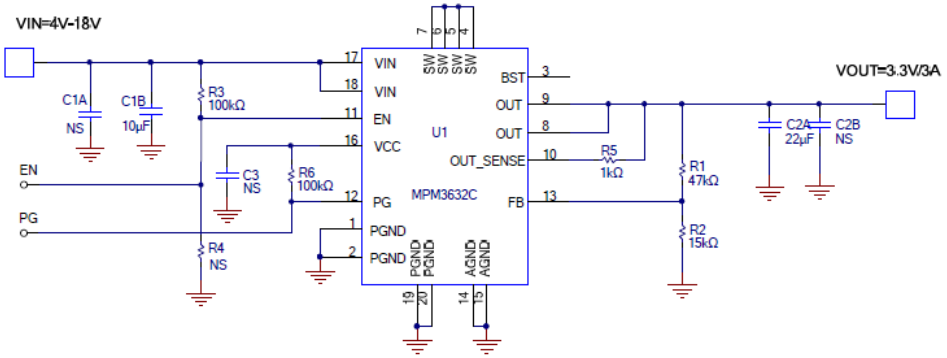
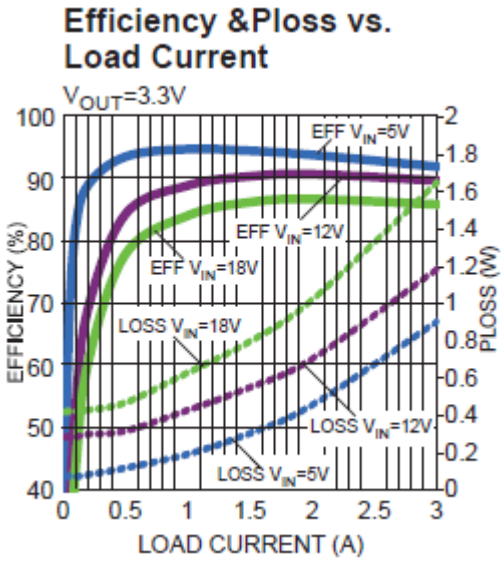
MPM3632C

Schematics





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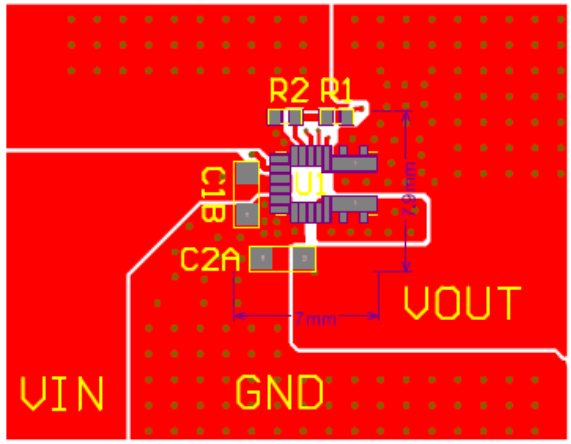
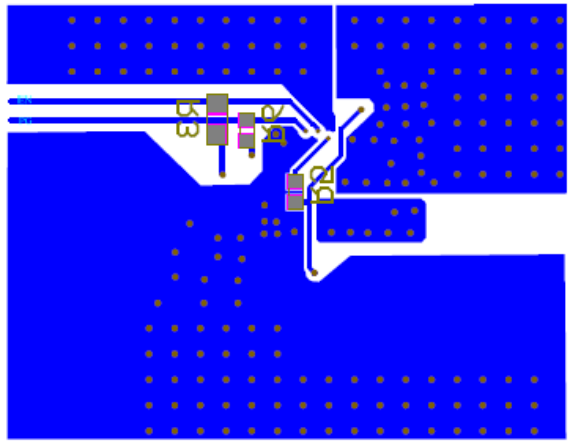


Top Layer



PCB area 55mm2

Caps included in area calculations:

Output Caps 1x 22uF 0805

Input Caps: 2x 0603 on PCB bottom

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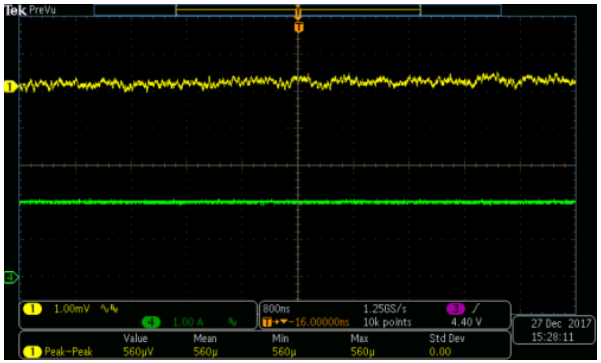
Analog rails – Expected ripple performance based on MPM3833C (EVREF102-A)

ADC_AVCC

Vo=0.925V,I_o=2A

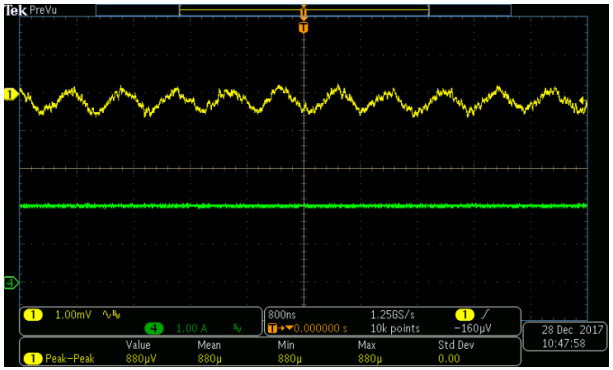
$V_{o,P-P}$=0.56mV



ADC_AVCCAUX

Vo=1.8V,I_o=2A

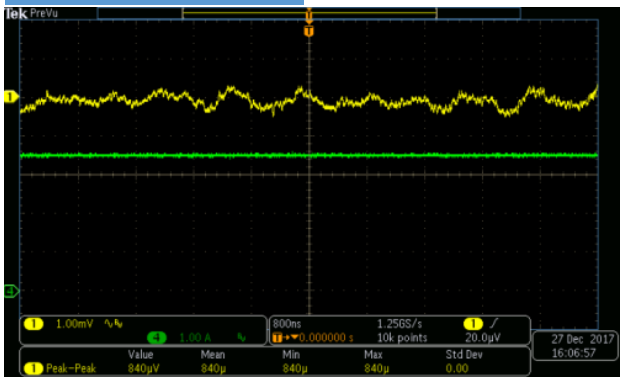
$V_{o,P-P}$=0.88mV



DAC_AVCC

Vo=0.925V,I_o=3.5A

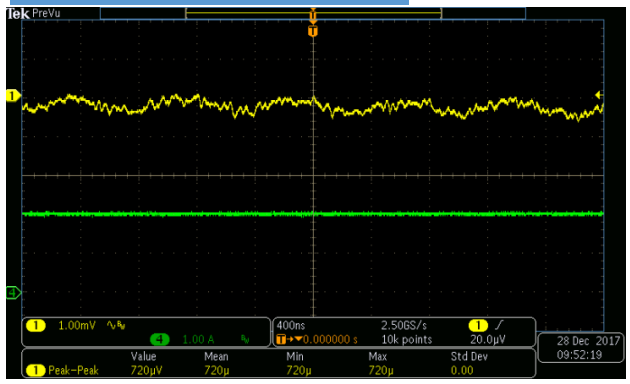
$V_{o,P-P}$=0.84mV



DAC_AVCCAUX

Vo=1.8V,I_o=2A

$V_{o,P-P}$=0.72mV



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MPS Support

MPS support for Xilinx customers

- Engineering support for design reviews, bring up and debug
- Our FAEs can assist with optimizing reference designs for customer's exact requirements
- MPS already working with leading SoC vendors and have support teams already in place for reference designs
- Power FAEs located in all major territories for world wide support

Simulation tools:

- Models available for predicting Efficiency, Power loss, Load step response, Phase margin and other key requirements.

Evaluation

- EVBs available
- MPS can provide free samples for evaluation and prototyping

MPS contact Thomas.fenn@monolithicpower.com

MPS Reference Design Team at referencedesign@monolithicpower.com

For general information
http://www.monolithicpower.com

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